CLAIMS:

1. A semiconductor processing method of forming field effect transistors comprising:

forming a first gate dielectric layer over first and second areas of a semiconductor substrate, the first area being configured for forming p-type field effect transistors, the second area being configured for forming n-type field effect transistors;

removing the first gate dielectric layer from over one of the first and second areas and leaving the first gate dielectric layer over the other of the first and second areas;

after the removing, forming a second gate dielectric layer over the other of the first and second areas;

forming transistor gates over the first and second gate dielectric layers; and

forming p-type source/drain regions proximate the transistor gates in the first area and n-type source/drain regions proximate the transistor gates in the second area.

2. The semiconductor processing method of claim 1 wherein the removing comprises removing the first gate dielectric layer from over the first area.

3. The semiconductor processing method of claim 1 wherein the removing comprises removing the first gate dielectric layer from over the second area.

4. The semiconductor processing method of claim 1 wherein the first gate dielectric layer is different in composition relative the second gate dielectric layer.

5. The semiconductor processing method of claim 1 wherein the first gate dielectric layer is of a different thickness relative the second gate dielectric layer.

6. The semiconductor processing method of claim 1 wherein the first gate dielectric layer is different in composition and is of a different thickness relative the second gate dielectric layer.

7. The semiconductor processing method of claim 1 wherein the first gate dielectric layer comprises an oxide having nitrogen atoms therein, the nitrogen atoms being higher in concentration within the first gate dielectric layer at one elevational location as compared to another elevational location, and the second gate dielectric layer being different in composition from the first gate dielectric layer.

8. The semiconductor processing method of claim 1 wherein the first gate dielectric layer comprises an oxide having nitrogen atoms therein, the nitrogen atoms being concentrated within the first gate dielectric layer at a location proximate an interface of the first gate dielectric layer with the semiconductor substrate, and the second gate dielectric layer being different in composition from the first gate dielectric layer.

9. The semiconductor processing method of claim 1 wherein the first gate dielectric layer comprises silicon dioxide having nitrogen atoms therein, the nitrogen atoms being higher in concentration within the first gate dielectric layer at one elevational location as compared to another elevational location and at a concentration of from 0.1% molar to 10.0% molar, and the second gate dielectric layer comprises silicon dioxide material proximate an interface of the second gate dielectric layer with the semiconductor substrate which is substantially void of nitrogen atoms.

10. The semiconductor processing method of claim 1 wherein the first gate dielectric layer comprises an oxide.

11. The semiconductor processing method of claim 1 wherein the second gate dielectric layer comprises an oxide.

12. A semiconductor processing method of forming field effect transistors comprising:

forming a first gate dielectric layer over first and second areas of a semiconductor substrate, the first area being configured for forming p-type field effect transistors, the second area being configured for forming n-type field effect transistors, the first gate dielectric layer comprising silicon dioxide having nitrogen atoms therein, the nitrogen atoms being higher in concentration within the first gate dielectric layer at one elevational location as compared to another elevational location and at a concentration of from 0.1% molar to 10.0% molar;

removing the first gate dielectric layer from over the second area and leaving the first gate dielectric layer over the first area;

after the removing, forming a second gate dielectric layer over the second area, the second gate dielectric layer comprising silicon dioxide proximate an interface of the second gate dielectric layer with the semiconductor substrate which is substantially void of nitrogen atoms;

forming transistor gates over the first and second gate dielectric layers; and

forming p-type source/drain regions proximate the transistor gates in the first area and n-type source/drain regions proximate the transistor gates in the second area.

13. The semiconductor processing method of claim 12 wherein the one elevational location is located proximate an interface of the first gate dielectric layer with the semiconductor substrate.

14. The semiconductor processing method of claim 12 wherein the second gate dielectric layer is formed to at least initially cover all of the first and second areas.

15. The semiconductor processing method of claim 12 wherein the second gate dielectric layer is formed to at least initially cover a majority of the second area.

16. The semiconductor processing method of claim 12 wherein the second gate dielectric layer is formed to at least initially cover only the second area.

17. The semiconductor processing method of claim 12 wherein the first gate dielectric layer is of a different thickness relative the second gate dielectric layer.

18. A semiconductor processing method of forming field effect transistors comprising:

forming a first gate dielectric layer over a first area of a semiconductor substrate configured for forming p-type transistors and a second gate dielectric layer over a second area of the semiconductor substrate configured for forming n-type transistors, the first gate dielectric layer comprising an oxide having nitrogen atoms therein, the nitrogen atoms being higher in concentration within the first gate dielectric layer at one elevational location as compared to another elevational location, the second gate dielectric layer being different in composition from the first gate dielectric layer;

forming transistor gates over the first and second gate dielectric layers; and

forming p-type source/drain regions proximate the transistor gates in the first area and n-type source/drain regions proximate the transistor gates in the second area.

19. The semiconductor processing method of claim 18 wherein the one elevational location is located proximate an interface of the first gate dielectric layer with the semiconductor substrate.

20. The semiconductor processing method of claim 18 wherein the concentration of nitrogen atoms within the first gate dielectric layer at the one elevational location is from 0.1% molar to 10.0% molar.

21. The semiconductor processing method of claim 18 wherein the first gate dielectric layer is formed before the second gate dielectric layer.

22. The semiconductor processing method of claim 18 wherein the second gate dielectric layer is formed before the first gate dielectric layer.

23. The semiconductor processing method of claim 18 wherein the first gate dielectric layer comprises silicon dioxide.

24. The semiconductor processing method of claim 18 wherein the first gate dielectric layer is of a different thickness relative the second gate dielectric layer.

25. The semiconductor processing method of claim 18 wherein the first gate dielectric layer is initially formed over the first and second areas.

26. The semiconductor processing method of claim 18 wherein the second gate dielectric layer is initially formed over the first and second areas.

27. Integrated circuitry comprising a semiconductor substrate having an area within which a plurality of n-type and p-type field effect transistors are formed, the respective transistors comprising a gate, a gate dielectric layer and source/drain regions, the gate dielectric layer of the p-type field effect transistors comprising an oxide having nitrogen atoms therein, and the nitrogen atoms being higher in concentration within the gate dielectric layer at one elevational location as compared to another elevational location, the gate dielectric layer of the n-type field effect transistors being different in composition from the gate dielectric layer of the p-type field effect transistors.

28. The integrated circuitry of claim 27 wherein the gate dielectric layer of the p-type transistors comprises silicon dioxide.

29. The integrated circuitry of claim 27 wherein the gate dielectric layer of the p-type transistors are of a different thickness relative the gate dielectric layer of the n-type transistors.

30. The integrated circuitry of claim 27 wherein the concentration of nitrogen atoms in the gate dielectric layer of the p-type transistors at the one elevational location is from 0.1% molar to 10.0% molar.

31. The integrated circuitry of claim 27 wherein the one elevational location is located proximate an interface of the gate dielectric layer with the semiconductor substrate.

32. Integrated circuitry comprising a semiconductor substrate having an area within which a plurality of n-type and p-type field effect transistors are formed, the respective transistors comprising a gate, a gate dielectric layer and source/drain regions, the gate dielectric layer of the p-type field effect transistors comprising silicon dioxide having nitrogen atoms therein, the nitrogen atoms being higher in concentration within the gate dielectric layer at one elevational location as compared to another elevational location and at a concentration of from 0.1% molar to 10.0% molar, the gate dielectric layer of the n-type field effect transistors comprising silicon dioxide material proximate an interface of the gate dielectric layer with the semiconductor substrate which is substantially void of nitrogen atoms.

33. The integrated circuitry of claim 32 wherein the one elevational location is located proximate an interface of the gate dielectric layer with the semiconductor substrate.

34. A semiconductor processing method of forming field effect transistors comprising:

providing a continuous area over a semiconductor substrate for formation of n-type and p-type field effect transistors, the transistors respectively comprising a gate, a gate dielectric layer and source/drain regions; and

forming a predominate portion of the gate dielectric layers of the p-type transistors in the first continuous area prior to forming a predominate portion of the gate dielectric layers of the n-type transistors in the first continuous area.

35. The semiconductor processing method of claim 34 wherein the gate dielectric layer of the p-type transistors comprise an oxide having nitrogen atoms therein, the nitrogen atoms being higher in concentration within the gate dielectric layer at one elevational location as compared to another elevational location.

36. The semiconductor processing method of claim 34 wherein the gate dielectric layer of the p-type transistors comprise an oxide having nitrogen atoms therein, the nitrogen atoms being concentrated within the gate dielectric layer at a location proximate an interface of the gate dielectric layer with the semiconductor substrate.

37. The semiconductor processing method of claim 34 wherein the gate dielectric layer of the p-type transistors comprise an oxide having nitrogen atoms therein and located proximate an interface of the gate dielectric layer with the semiconductor substrate at a concentration from 0.1% molar to 10.0% molar.